Amendments to and Listing of the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 1-32 remain in this application.

Claims 1-3 and 16 are being amended.

Claims 4, 5, 21, 22 are original.

Claims 6-15, 17-20 and 23-32 are being canceled.

WHAT IS CLAIMED IS:

1. (Currently Amended) An integrated circuit for electrostatic discharge (ESD) protection comprising:

~~(a)~~ a silicon-controlled rectifier (SCR) including [[:]]

~~(i)~~ a first transistor ~~of a first type~~ integrally formed with the SCR, wherein the first transistor has ~~including~~ a first gate located over a channel between a first doped region of the SCR and a second doped region of the SCR ~~, and~~

~~(ii) a second transistor of a second type integrally formed with the SCR including a second gate~~;

a contact pad coupled to the SCR; ~~and~~

~~(b)~~ a control circuit coupled to the silicon-controlled rectifier, wherein the control circuit changes ~~in response to a first voltage applied to the first and second gates providing~~ a ~~first~~ normal holding voltage of ~~to~~ the SCR to a modified holding voltage to keep the SCR in latch-up ~~from latching up~~ after detecting a electronic static discharge event, and changes ~~in response to a second voltage applied to the first and second gates providing a second~~ the modified holding voltage of ~~to~~ the SCR to the normal holding voltage after a time period to keep the SCR from latching up ~~in the latch-up state~~; and

wherein the first gate of the first transistor is not directly coupled to the control circuit.

2. (Currently Amended) The circuit of claim 1, wherein the time period is determined by an RC constant of the control circuit.~~the control circuit further comprising an output terminal coupled to the first and second gates.~~

3. (Currently Amended) The circuit of claim 1, the control circuit further comprising a resistor, a capacitor and an output terminal of the control circuit disposed between the resistor and the capacitor.

4. (Original) The circuit of claim 1, the control circuit including a resistor-capacitor delay circuit.

5. (Original) The circuit of claim 1, the SCR further comprising a p-type substrate, an n-well formed in the p-type substrate, a p-type diffused region formed in the n-well, and an n-type diffused region formed outside of the n-well.

6 – 15. (Canceled)

16. (Currently Amended) An integrated circuit for electrostatic discharge (ESD) protection comprising:

~~a first voltage line of a first voltage level;~~

~~a second voltage line of a second voltage level;~~

a plurality of contact pads;

a plurality of first silicon-controlled rectifiers (SCR), each of the first SCRs associated with one of the plurality of contact pads, wherein each first SCR includes ~~including~~ a ~~p-type~~ first MOS transistor ~~and an n-type transistor~~ integrally formed with the SCR;

wherein for each of the first SCRs, a gate of the first MOS transistor is coupled to the contact pad or ground; and

a plurality of control circuits, wherein a control circuit coupled to each of the first SCRs, wherein the control circuit changes a normal holding voltage of the SCR to a modified holding voltage to keep the SCR in latch-up after detecting an electrostatic discharge event, and changing

the modified holding voltage of the SCR to a normal holding voltage after a time period to keep the SCR from latching up. ~~providing a first holding voltage through the p-type and n-type transistors to the SCRs to keep the SCRs from latching-up, and providing a second holding voltage through the p-type and n-type transistors to the SCRs to keep the SCRs in the latch-up state during an ESD event that an ESD pulse appears on the first voltage line or one of the contact pads~~.

17-20. (Canceled)

21. (Original) The circuit of claim 16, each control circuit further comprising a resistor-capacitor delay circuit.

22. (Original) The circuit of claim 16, each control circuit further comprising an output terminal coupled to a gate of each of the p-type and n-type transistors.

23-32. (Canceled)